CLAIMS

1. A fail-safe system for differential current logic receiver circuits, wherein a fail-safe condition includes receiver inputs that are,floating, undriven, shorted together, or one or both shorted to ground, the fail-safe system comprising:

a current mode differential receiver defining first and second inputs,

a first driver of current into the first input and a second driver of current into the second input, wherein the first and the second currents are not equal to each other under normal operation,

means for sensing the unequal currents and outputting a differential current corresponding to the received unequal currents, wherein in any defined fail-safe conditions the differential current output of the means for sensing remains stable.

2. The fail-safe system of claim 1 wherein the means for sensing comprises:

means for establishing a differential current threshold wherein when the threshold is reached the means for sensing outputs a changed logic state.

3. The fail-safe system of claim 1 further comprising:

a differential current amplifier arranged to accept the differential current output of the means for sensing and provide an amplified current, and

a current to voltage converter that accepts the amplified current and outputs a voltage signal consistent with logic system.

4. The fail-safe system of claim 1 further comprising a resistor connected between the first and the second inputs.

5. The fail-safe system of claim 1 wherein the means for sensing comprises:

a first current receiving circuit connected between the first input and a current return path back to the current drivers,

a second current receiving circuit connected between the second input and a current return path back to the current drivers.

6. The fail-safe system of claim 5 wherein the first and second current receiving circuits comprise diode connected MOS transistors.

7. The fail-safe system of claims 6 further comprising means for biasing each diode connected MOS transistor so that each presents a given impedance to a current return path to the current drivers.

8. The fail-safe system of claim 5 further comprising means for comparing the currents in the first receiving circuit to the current in the second receiving circuit.

9. The fail-safe system of claim 8 wherein the means for comparing comprise:

a first amplifying current mirroring circuit providing a first mirrored output current of the current received by the first receiving circuit,

a second amplifying current mirroring circuit providing a second mirrored output current of the current received by the second receiving circuit, and

a current to voltage conversion circuit, arranged to receive the first and the second output currents and provide a voltage output that is proportional to the difference between the outputs of the first and the second amplifying current mirroring circuits.

10. A method for generating a fail-safe condition system for differential current logic receiver circuits when receiver inputs are: floating, undriven, shorted together, or one or both shorted to ground, the method comprising the steps of:

receiving external differential noise currents with a current mode differential receiver defining first and second inputs,

driving a first current into the first input and a second current into the second input, wherein the difference between external current noise on differential data lines is

usually not big enough to overcome the threshold set by the failsafe bias transistors internally under failsafe condition,

sensing the unequal currents efficiently while under normal operation, and

outputting a stable known state while under fail-safe conditions.